

### AMENDMENTS TO THE CLAIMS

Please cancel claims 10 and 15-18 and amend claims 1-9 and 11-14 as set forth below.

1. (CURRENTLY AMENDED) A semiconductor memory apparatus comprising:

a memory unit having a plurality of unit blocks, wherein each unit block including includes:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein[[:] ]

said plurality of unit blocks ~~are further laid out to form a block matrix or a plurality of block matrixes, and every~~ each of said plurality of said-unit blocks forms a one-dimensional group oriented in a first direction (row or column direction) or a second direction (column or row direction); and

said redundant lines are shared by a group of said plurality of unit blocks ~~pertaining to, wherein the group of said plurality unit blocks have a common orientation of~~ said one-dimensional group;

self-test means for evaluating said memory cells to determine whether said memory cells are abnormal, wherein said self-test means is mounted in the same chip as said memory unit ~~to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective; and~~

self-repair means for receiving address pairs associated with an abnormal memory cell from said self-test means, mounted in said same chip as said memory unit to serve as embedded self-repair means for:

selecting ~~only a minimum number of address pairs among of the plurality of~~ address pairs received from said ~~embedded self-test means as address pairs- means, wherein each address pair including a~~ includes a first-direction address (row or column address) and a second-direction address (column or row address) of an-associated with the abnormal memory cell; cell,

storing said selected minimum number of address pairs in first storage means for each of said plurality of unit blocks as address-pairs required for determining to determine a redundant line to be used ~~for repairing an~~ to repair the abnormal memory cell; and

finding a redundant line to ~~be used for repairing an~~ repair the abnormal memory cell ~~for each of said unit blocks on the basis of~~ based on address pairs stored in said first storage means.

2. (CURRENTLY AMENDED) A ~~The~~ semiconductor memory apparatus according to claim 1, wherein:

said ~~embedded~~ self-repair means has a first storage unit and a first shift-register unit;

said first storage unit is capable of storing a maximum number of ~~possible different~~ second-direction addresses selected from ~~the~~ address pairs stored in said first storage means for ~~all~~ each unit block in said group of unit blocks ~~pertaining to of~~ said one-dimensional group ~~on the assumption that said group, wherein each unit blocks form forms~~ said one-dimensional group commonly oriented in said second direction and said redundant lines connected in said second direction are shared by ~~said each unit blocks block pertaining to of~~ said one-dimensional group;

said first shift-register unit has ~~as many a~~ plurality of shift ~~registers~~ registers, wherein the number of the plurality of shift registers equals the number of said redundant lines connected in said second direction;

each of said shift registers has as many shift stage bits as said maximum number; and

said first shift-register unit sequentially points to one of said second-direction addresses stored in said first storage unit by shifting ~~said the~~ plurality of shift registers; and

said first shift-register unit generates ~~a pattern of~~ an address set of said second-direction address for each unit block by operating only one of said plurality of shift registers at a time.

3. (CURRENTLY AMENDED) A ~~The~~ semiconductor memory apparatus according to claim 2, wherein:

~~an~~ the address set generated as an address set of a second-direction address is reported for ~~all said unit blocks~~ each unit block and, if ~~an~~ the address pair including said second-direction address exists in said first storage means, said address pair is ~~assumed to be~~ an address pair that can be repaired by using a redundant line connected in said second direction; and

if an address pair ~~remains~~remaining in said first storage means as ~~an unrepairable address pair to be repaired~~is unrepaired, said remaining address pair ~~remaining to be repaired~~ is examined to determine whether ~~or not said unrepairable~~said remaining address pair ~~remaining to be repaired can be repaired~~is repairable by using a redundant line connected in said first direction.

4. (CURRENTLY AMENDED) A- The semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether or not it is possible to use a redundant line connected in said first direction for repairing ~~a~~the remaining address pair, ~~which pair that~~ cannot be repaired by using a redundant line connected in said second direction, said ~~embedded~~ self-repair means ~~is provided with as many second storage units~~includes a plurality of second storage units that store a first-direction address, wherein a number of said second storage units equals a number of as said redundant lines connected to each unit block in said first direction ~~for each of said unit blocks as second storage units each used for storing a first direction address;~~ and

said ~~embedded~~ self-repair means executes the steps of:

supplying a first-direction address of ~~a~~the remaining address pair ~~which~~that cannot be repaired by using a redundant line connected in said second direction to said second storage units;

discarding said first-direction address of said remaining address pair ~~if~~when said first-direction address has already been stored in said second storage units;

determining that said remaining address pair can be repaired by using a redundant line connected in said first direction ~~if~~when said first-direction address ~~thereof can be accommodated~~is stored in said second storage units; and

determining that said remaining address pair cannot be repaired by using a redundant line connected in said first direction ~~if~~when said first-direction address ~~thereof cannot be accommodated~~is not stored in said second storage units.

5. (CURRENTLY AMENDED) A-The semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether ~~or not~~ it is possible to use a redundant line connected in said first direction for repairing a- the remaining address pair, which pair that cannot be repaired by using a redundant line connected in said second direction, said ~~embedded~~ self-repair means is provided with a plurality of first-direction shift registers wherein the number of first-direction shift registers corresponds to the number of redundant lines connected to each of said unit blocks in said first direction ~~as many first-direction shift registers independent of each other as said redundant lines connected in said first direction for each of said unit blocks;~~ and

said ~~embedded~~ self-repair means executes the steps of:

shifting ~~any~~ at least one of said first-direction shift registers and taking a first-direction address pointed to by said first-direction shift registers as a first-direction repair address;

determining whether ~~or not a~~ the remaining address pair, which pair that cannot be repaired by using a redundant line connected in said second direction, can be repaired by using a redundant line connected in said first direction as a redundant line corresponding to said first-direction repair address; and

further shifting ~~any~~ at least one of said first-direction shift registers and determining whether ~~or not~~ said remaining address pair can be repaired if said remaining address pair cannot be repaired by using said redundant line connected in said first direction.

6. (CURRENTLY AMENDED) A-The semiconductor memory apparatus according to claim 2, wherein said shift registers of said first shift-register unit each have ~~not only as many shift stage bits as said possible different second-direction addresses but also~~ an additional shift stage bit ~~for indicating~~ that indicates a state in which ~~no~~ redundant lines connected in said second direction are ~~used~~ ignored.

7. (CURRENTLY AMENDED) A- The semiconductor memory apparatus according to claim 2, wherein:

wherein the a-plurality of said shift registers employed in said first shift-register unit ~~are named~~ include at least a first shift register, a second shift register, and a third register and so on; register,

wherein with when said first shift register is fixed, ~~after said second shift register, said third shift register and so on are shifted following a shift in said second shift register and said third shift register,~~ said first shift register is shifted by 1 bit ~~and, after said first shift register is shifted by 1 bit,~~ and an operation to shift said second shift register is started from a shift-stage position coinciding with a new shift-stage position of said first shift register or a shift-stage position immediately following said new shift-stage position of said first shift register, and an operation to shift said third shift register is started from a shift-stage position coinciding with said start shift-stage position of said second shift register or a shift-stage position immediately following said start shift-stage position of said second shift register.

8. (CURRENTLY AMENDED) A The semiconductor memory apparatus according to claim 1, ~~wherein:~~

~~on the assumption that~~ wherein each of said unit blocks form block forms a one-dimensional group in said second direction, and said first storage means includes a plurality of shift register flags associated with the address pairs stored in said first storage means, wherein the number of as many shift-register flags as corresponds to the number of said redundant lines connected to each unit block commonly oriented in said second direction of in said second direction are provided for each of address pairs storable in said first storage means provided for all said unit blocks pertaining to said one-dimensional group;

wherein said plurality of shift-register flags are linked to each other to form as many shift registers each having a chain form spread over all said each unit blocks block as said redundant lines connected in said second direction;

wherein said plurality of shift registers form a second shift-register unit; and

wherein an address set of said second-direction address is generated by successively shifting each shift register of said plurality of shift registers of said second shift-register unit one register after another.

9. (CURRENTLY AMENDED) A The semiconductor memory apparatus according to claim 8, wherein said plurality of shift registers of said second shift-register unit ~~each have not~~

~~only as many shift stage bits as said address pairs storable for all said unit blocks pertaining to said one-dimensional group, but also~~ have an additional shift stage bit for indicating that  
indicates a state in which no-redundant lines connected in said second direction are used ignored.

10. (CANCELED)

11. (CURRENTLY AMENDED) A-The semiconductor memory apparatus according to claim 8, wherein:

wherein said ~~embedded-self-repair~~ means has a duplication flag ~~provided for~~ associated with each address pair of the plurality of address pairs ~~storable- stored~~ in said first storage means ~~provided for all said unit blocks~~;

wherein said duplication flags ~~are each used to indicate that an address pair associated with said duplication flag~~ a corresponding address pair includes a second-direction address stored ~~at 2 or more storage locations in~~ in at least two storage locations of said first storage means; and

wherein when ~~any particular~~ at least one of said plurality of shift registers ~~employed in~~ of said second shift-register unit is shifted to a next shift stage position coinciding with one of said duplication flags, which have been put in a set state, said next shift stage position is ignored and said particular shift register is shifted again.

12. (CURRENTLY AMENDED) A ~~The~~ semiconductor memory apparatus according to claim 11, wherein:

said ~~embedded~~ self-repair means reports a second-direction address pointed to by said shift registers ~~employed in of~~ said second shift-register unit for ~~all of said each~~ unit blocks block; and

~~if when~~ said reported second-direction address exists ~~also in~~ said first storage means for ~~another one of at least two of~~ said unit blocks, said duplication flag of ~~said other unit block~~ one of said at least two unit blocks is set.

13. (CURRENTLY AMENDED) A ~~The~~ semiconductor memory apparatus according to claim 8, wherein:

said ~~embedded~~ self-repair means reports to each unit block a second-direction address pointed to by said second shift-register unit ~~for all of said unit blocks~~ while shifting said second shift-register unit;

~~if when the same a duplicate~~ second-direction address ~~as of~~ said reported second-direction address ~~already exists in~~ said first storage means, said ~~embedded~~ self-repair means ~~assumes~~ determines that an address pair including said same second-direction address is a repairable address pair;

said ~~embedded~~ self-repair means first determines whether or not a remaining address pair, ~~if any, can be repaired~~ is repairable; and

said embedded self-repair means again shifts said second shift-register unit and again determine whether said remaining address pair are repairable if when a remaining address pair cannot be repaired based on the first determination, said embedded self repair means again shifts said second shift register unit and again determine whether or not said remaining address pair can be repaired.

14. (CURRENTLY AMENDED) A-The semiconductor memory apparatus according to claim 8, wherein said ~~embedded~~ self-repair means has a special flag ~~provided for each of each~~ address pair of the plurality of address pairs storable pairs of each unit block stored in said first storage means ~~for all of said unit blocks as a flag to be set to indicate that a second-direction~~ address of ~~an~~ at least one address pair associated with said special flag matches an address set of ~~a~~ the second-direction address reported by said embedded self-repair means ~~for all of said unit blocks each unit block and the at least one address pair is thus~~ regarded as a second-direction repair address.

Claims 15-18 are CANCELED.